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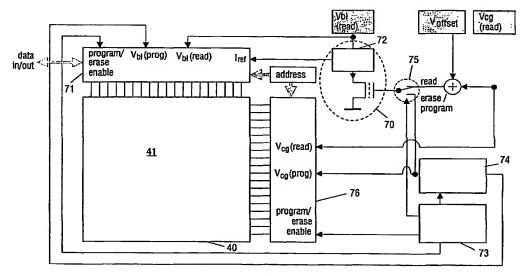
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(54) Title: IMPROVED ERASE AND READ SCHEMES FOR CHARGE TRAPPING NON-VOLATILE MEMORIES



(57) Abstract: The present invention describes a method for operating an array of nonvolatile charge trapping memory devices. The method comprises before a block erase step (52) of substantially all of the non-volatile memory devices of the array, block programming (51) of substantially all of the non-volatile memory devices of the array. It is an advantage of the present invention that, by doing this, a further charge trapping nonvolatile memory device may be used as a reference cell, which is programmed and erased with the block-programming and block-erasing of the memory cells in the array, so that the reference cell shows the same cycling history as the memory cells in the array. This feature can be used for adapting read parameters to ageing of the memory cells. Corresponding devices are also provided.

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